

03-2103

U.S. UTILITY PATENT APPLICATION

2681

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03-2703

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
(Attorney Docket No. BP 1904)

In the Application of:  
Oscar E. Agazzi  
App. Ser. No.: 10/086,267  
Filed: March 1, 2002 (03/01/2002)  
For: Digital signal processing based de-serializer

§ Group Art Unit: 2681  
§ Examiner: not yet assigned  
§ Confirmation No.: 4805

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Commissioner for Patents  
Washington, D.C. 20231

Technology Center 2600

Dear Sir or Madam:

It is requested that the enclosed reference(s) listed on the attached Information Disclosure Statement by Applicant (Form PTO/SB/08A (1 page) and Form PTO/SB/08B (2 pages)) be considered by the Patent Examiner in connection with the above-identified application and be made of record therein. In addition to the three (3) patent documents identified by the International Search Report Communication that is provided and referenced below, twelve (12) non-patent literature documents are provided independently by the Applicant.

**Certification Under 37 C.F.R. § 1.97(e)(1)**

I hereby certify that the corresponding enclosed reference(s) were cited in an International Search Report Communication (copy enclosed) dated February 18, 2003 (02/18/2003) from the U.S. Patent Office concerning counterpart International Application No. PCT/US 02/06414 (Attorney Docket No. BP 1904 PCT), not more than three months prior to the filing of this Information Disclosure Statement by Applicant.

Independent consideration and acknowledgment of the enclosed references is respectfully requested.

Respectfully submitted,

Date: March 20, 2003

By:

Shayne X. Short, Ph.D., Reg. No. 45,105  
USPTO Customer No. 34,399

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PTO/SB/08A (02-03)

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Approved for use through 07/06/2001 GPO:2001-000-0001-0001

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## **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

*(Use as many sheets as necessary)*

Sheet 1 of 3

<i><b>Complete if Known</b></i>	
Application Number	10/086,267
Filing Date	03/01/2002
First Named Inventor	Oscar E. Agazzi
Art Unit	2681
Examiner Name	n/a
Attorney Docket Number	BP 1904

## **U. S. PATENT DOCUMENTS**

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## **FOREIGN PATENT DOCUMENTS**

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear
		Country Code <sup>3</sup> -Number <sup>4</sup> -Kind Code <sup>5</sup> (if known)			
		EP 1 006 697 A2	06-07-2000	Kameran Azadet	
		EP 0 617 521 A2	09-28-1994	Zoran Kostic	

<b>Examiner Signature</b>		<b>Date Considered</b>	
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Attorney Docket Number	BP 1904

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### OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS

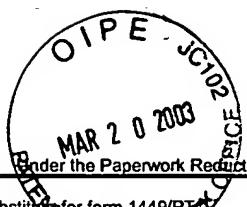
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		W. Ellersick, C. K. Yang, M. Horowitz, and W. Dally, "GAD: A 12GS/s CMOS 4-bit A/D Converter for an Equalized Multi-Level Link," 1999 Symposium on VLSI Circuits, pp. 49-52.	
		W. Ellersick, C. K. Yang, V. Stojanovic, S. Modjtahedi, and M. A. Horowitz, "A Serial-Link Transceiver Based on 8Gsmpale/s A/D and D/A Converters in 0.25 um CMOS," 2001 IEEE International Solid-State Circuits Conference, San Francisco, February 2001, 3 pages.	
		C. K. Yang, V. Stojanovic, S. Modjtahedi, M. A. Horowitz, and W. F. Ellersick, "A Serial-Link Transceiver Based on 8Gsmpale/s A/D and D/A Converters in 0.25 um CMOS," IEEE Journal of Solid-State Circuits, Vol.36, No.11, November 2001, pp. 1684-1692.	
		C. S. G. Conroy, D. W. Cline, and P. R. Gray, "An 8-b 85MS/s Parallel Pipeline AID Converter in 1 um CMOS," IEEE Journal of Solid-State Circuits, Vol.28, No.4, April 1993, pp. 447-454.	
		J-E. Eklund and F. Gustafsson, "Digital Offset Compensation of Time-Interleaved ADC Using Random Chopper Sampling," International Symposium on Circuits and Systems, May 28-31, 2000, Geneva, Switzerland, pp. III-447-III-450.	
		Y-C. Jenq, "Digital Spectra of Nonuniformly Sampled Signals: A Robust Sampling Time Offset Estimation Algorithm for Ultra High-Speed Waveform Digitizers Using Interleaving," IEEE Transactions on Instrumentation and Measurements, Vol.39, No.1, February 1990, pp. 71-75.	
		D. Fu, K. C. Dyer, S. H. Lewis, and P. J. Hurst, "A Digital Background Calibration Technique for Time-Interleaved Analog-to-Digital Converters," IEEE Journal of Solid-State Circuits, Vol.33, No.12, December 1998, pp. 1904-1911.	
		C. K. Yang, "Design Techniques for High-Speed Chip-to-Chip Links," <a href="http://web.doe.carleton.ca/courses/97578/topic5/Tutorial_SerialLink.pdf">http://web.doe.carleton.ca/courses/97578/topic5/Tutorial_SerialLink.pdf</a> , 31 pages.	
		W. J. Dally and J. Poulton, "Transmitter Equalization for 4Gb/s Signalling," Proceedings of Hot Interconnects IV, Palo Alto, 1996, 10 pages.	
		W. C. Black and D. A. Hodges, "Time Interleaved Converter Arrays," IEEE Journal of Solid-State Circuits, Vol.SC-15, No.6, December 1980, pp. 1022-1029.	

Examiner Signature	Date Considered
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## **INFORMATION DISCLOSURE STATEMENT BY APPLICANT**

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Sheet 3 of 3 Attorney Docket Number BP 1904

## **OTHER PRIOR ART-NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		A. Petraglia and S. K. Mitra, "Analysis of Mismatch Effects Among A/D Converters in a Time-Interleaved Waveform Digitizer," IEEE Transactions on Instrumentations and Measurements, Vol.40, No.5, October 1991, pp. 831-835.	
		S. Kasturia and J. H. Winters, "Techniques for High-Speed Implementation of Nonlinear Cancellation," IEEE Journal on Selected Areas in Communications, Vol.9, No.5, June 1991, pp. 711-717.	
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